EE / CprE / SE 4920 – sdmay26-12
ABC with Modern Components
Report 10

01/20/2026 – 02/05/2026
Client: Alexander Stoytchev
Faculty Advisor: Alexander Stoytchev

Team Members:

Gavin Bunker — *Technical Manual Lead*
Ryan McFadden — *Client Liaison, Recorder*
Samuel Schroeder — *Team Leader*
Vance Arnold — *Team Facilitator, Purchasing*
Bryan York — *PCB Lead*
Kyle Koch — *VHDL Lead*

Summary

This reporting period saw us finish up a few of the modules that were nearing completion at the end of last semester. In particular, the base conversion module was assembled and tested, and the decimal output module was finalized and ordered. Additionally, work continued on the design of the PC/clock and control modules. Significant progress was also made on the full software simulation of our ABC replica.

Past Weeks Accomplishments

- Kyle
  - Got the Adder/Subtractor file of the 5 add/subs made in VHDL and then converted to BSF files.
  - Sat down with Vance and got the entire BDF file for the ABC design, except for the EEPROM and instruction memory.
- Vance
  - Completed the RAM/drum VHDL modules and converted to BSF files.
  - Worked with Kyle to complete the entire BDF dataflow design for the ABC, with a few components pending future work.
- Samuel
  - Finalized and reviewed the PCB design for the decimal output module
  - Created a Python simulation to verify the correctness of the ABC's sign-change signal
  - Created logical designs for five of the six main control modules
- Bryan
  - Implemented design changes to the Output Display Module given to us by our advisor. Added solder pads to implement Atanassoff or Berry's versions
  - Sent output display to ETG for production
- Gavin
  - Redrew and reorganized the PC/clock module
  - Optimized PC/clock module to reduce chips required
  - Wrote a Java class as a descriptional representation of the PC/clock module

- Ryan
    - Soldered and tested Base Conversion Module Rev A
    - After finding an error in Rev A, I designed the Base Conversion Module Rev B

Pending Issues

- No pending issues

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Gavin Bunker	Organizing and optimizing the PC/clock Wrote a Java class as a descriptional representation of the PC/clock module	12	12
Ryan McFadden	Designed, soldered, and tested Base Conversion Module Rev A, designed Base Conversion Module Rev B	5	5
Samuel Schroeder	Review and support decimal output module, design and testing of control system	20	20
Vance Arnold	Designed individual VHDL modules for Dataflow (whiteboard figure), converted modules to symbols in Quartus for a BDF. Currently testing implementation	12	12
Bryan York	Designed and laid out a module for decimal output in KiCAD. Reviewed designs with team members and advisors	7	7
Kyle Koch	Worked with Vance on the VHDL design and conversion. Then helped with the layout of said units into BDF format and used it as we did in CprE 281.	10	10

Plans for Coming Weeks

- Kyle and Vance - Write VHDL for EEPROM and input cards, start simulation on FPGA
- Bryan - start designing PCB for memory drum and shifter
- Ryan - finish conversion drum Rev B, start designing control panel
- Samuel - finishing designing the control modules, start simulating them
- Gavin - Work on further documentation, make a parts list for the PC/clock module, and verify the footprints are accurate prior to PCB fabrication.