EE / CprE / SE 4920 – sdmay26-12
ABC with Modern Components
Report 11

02/06/2026 – 02/12/2026
Client: Alexander Stoytchev
Faculty Advisor: Alexander Stoytchev

Team Members:

Gavin Bunker — *Technical Manual Lead*
Ryan McFadden — *Client Liaison, Recorder*
Samuel Schroeder — *Team Leader*
Vance Arnold — *Team Facilitator, Purchasing*
Bryan York — *PCB Lead*
Kyle Koch — *VHDL Lead*

Summary

With the completion of the decimal output and decimal conversion modules during the last reporting period and the start of this period, our team began work on two new modules for our ABC recreation. All buttons, switches, and other I/O components from the original ABC's control panel were inventoried to begin creating the control panel, and work began on selecting appropriate chips and creating the schematic for the memory modules. Significant design and documentation work was completed for the in-progress control and clock modules, as well as the VHDL implementation of certain system components.

Past Weeks Accomplishments

- Gavin
  - Created a boolean table for the entire PC/clk module
  - Implemented additional desired changes to the module
  - Created an English description of the submodules
- Bryan
  - Looked through different chip options for the memory drum circuit.
  - Started schematic of memory drum circuit from the existing block diagram
- Samuel
  - Documented and completed designing all six of the main control modules, including a description of the module, how it works, inputs and outputs, and a design diagram
  - Reviewed Ryan's control panel inventory
  - Started designing and documenting the timing drum
- Kyle
  - Continued working on the memory and inputs of the VHDL design to allow for 4 masks and 3 equations as a way to verify our design works.
  - Worked with Vance a bit on the EEPROM to VHDL to make sure it works as expected.
- Vance
  - Continued work with Kyle on implementation of EEPROM in VHDL.
  - Continued work on the overall VHDL and Block Diagram of ABC, including fixing up dataflow (whiteboard figure) and input/output.

- Ryan
    - Worked with ETG to make sure RevB of our Base Conversion Module was successfully ordered
    - Created a spreadsheet detailing the I/O elements of the control panel

Pending Issues

- Bryan
    - There is still no good single-chip 5-bit multiplexer available on the market.

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Gavin Bunker	Documentation and design changes for the PC/clk	5	17
Ryan McFadden	Base Conversion module fabrication, created control panel spreadsheet	5	15
Samuel Schroeder	Control system design and documentation, control panel review	8	28
Vance Arnold	EEPROM VHDL research and work, Overall ABC VHDL and Block Diagram fixes and work including I/O	4	16
Bryan York	Design and chip selection for memory drums	10	17
Kyle Koch	Work on the Overall ABC VHDL and Block Diagram, and work with how we will do I/O for testing of the VHDL design	4	14

Plans for Coming Week

- Bryan
    - Continue to narrow in on which ICs will work for the memory drum
    - Read through all datasheets and specs to ensure all chips meet the specs of our system, and will communicate correctly with one another.
    - Solder and test the output display module once received from JLCPCB
- Vance
    - Complete EEPROM VHDL implementation
    - Decide on and complete an I/O representation for FPGA simulation and actual project
- Kyle
    - Complete EEPROM VHDL implementation
    - Decide on and complete an I/O representation for FPGA simulation and actual project
- Ryan
    - Discuss control panel spreadsheet with Dr. Stoytchev
    - Create a schematic for the control panel module
- Samuel
    - Finish design and documentation of the timing drum
    - Start designing the control table