EE / CprE / SE 4920 – sdmay26-12
ABC with Modern Components
Report 12

02/13/2026 – 02/26/2026
Client: Alexander Stoytchev
Faculty Advisor: Alexander Stoytchev

Team Members:

Gavin Bunker — *Technical Manual Lead*
Ryan McFadden — *Client Liaison, Recorder*
Samuel Schroeder — *Team Leader*
Vance Arnold — *Team Facilitator, Purchasing*
Bryan York — *PCB Lead*
Kyle Koch — *VHDL Lead*

Summary

During this reporting period, we completed much of the design work on the components previously under development and have begun moving into the verification and implementation phases for these modules. Specifically, the designs for the clock, control system, and memory drums were finalized, and they are now being tested in VHDL and converted into KiCAD schematics and PCB layouts. Revision B of the binary conversion module has also completed fabrication and testing. For the full VHDL simulation, testbench files and card reader systems have been implemented to easily provide test inputs to the simulation.

Past Weeks Accomplishments

Gavin

- Wrote >1000 lines of VHDL to test the clock module prior to fabrication
- Finalizing clock module wraparound and batching logic
- Further simplification of all things in the schematic and design
- Custom symbols and footprinting work
- Planned possible PSU implementations and tablet interfacing
- Chip parts research and datasheet-based VHDL writing and proofreading
- Studied how to solder a uSOP device

Ryan

- Researched the control panel and made a graphic for what each button, switch, LED, and bridge does. I updated the schematic accordingly and began working on the PCB layout for the control panel.
- Rev B of the Base Conversion Module came in, so I soldered on all of the components for it, and created a robust breadboard testbench to test all 5 of the EEPROMS at once with different inputs for the digits. It worked well.

Vance

- Finished two EEPROM files and testbench of all 10.24 million combinations. Tested with python script and manual testing.
- Created 7-to-1 mux, 16-to-1 mux, 1-to-16 demux, and 10-4 encoder in VHDL.
- Continued Block Diagram work. Added all new components and wired up, specifically furthering work on decimal card input of the block diagram for further FPGA use.

Bryan

- Finalized chip options for the memory drum PCB
- Finished laying out the first draft of the memory drum schematic in Kicad.
- Reviewed timing and enabled signals for memory RAM chips.
- Reviewed requirements for the power supply to the board.

Kyle

- Worked on a VHDL CSV parser that reads based on an input of a string from a 16-1 mux and stores into a local reg file that then outputs the 5 decades of the 5 different variables.
- Worked on an issue of how our design works and talked with our client and Samuel to fix the issue with shifting.
- Created a bunch of CSV files for the decimal cards and plan to work on the binary cards next.

Samuel

- Finalized and documented the design of the entire control system
- Selected the required chips for the control system
- Began creating the control system schematic in KiCAD

Pending Issues

- No pending issues

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Gavin Bunker	Wrote VHDL to test the clock module prior to fabrication, finalized clock module functionality and simplifications, planned possible PSU implementations, studied how to solder a uSOP device	18	35
Ryan McFadden	Researched control panel and worked on its schematic and PCB layout, soldered and tested Base Conversion RevB and created a breadboard testbench for it	18	33
Samuel Schroeder	Finished control system design and documentation, started on the PCB for it	10	38
Vance Arnold	Completed EEPROM VHDL, created multiple VHDL components, continued Block Diagram implementation	20	36
Bryan York	Designed and drafted the schematic for the memory chip. Started to layout the power supply module.	14	31
Kyle Koch	Worked on a CSV parser in VHDL and then worked on design issues and worked with Vance on.	18	32

Plans for Coming Week

- Kyle and Vance
    - Continue completion of decimal input VHDL and Block Diagram work
    - Move on to binary card implementation
    - Begin testing with easy equations

- Samuel
    - Continue creating the KiCAD schematic and VHDL simulation of the control system
- Ryan
    - Update the control panel with the nicer switches and buttons we received
    - Continue working on the control panel PCB layout
- Bryan
    - Reviewing and revising the memory drum schematic, start laying out the PCB for the memory drum
    - Work on the power supply board and the required power for the system
- Gavin
    - Finalize VHDL simulations and schematics for the clock
    - Start laying out the PCB for the clock