EE / CprE / SE 4920 – sdmay26-12
ABC with Modern Components
Report 13

02/27/2026 – 03/12/2026
Client: Alexander Stoytchev
Faculty Advisor: Alexander Stoytchev

Team Members:

Gavin Bunker — *Technical Manual Lead*
Ryan McFadden — *Client Liaison, Recorder*
Samuel Schroeder — *Team Leader*
Vance Arnold — *Team Facilitator, Purchasing*
Bryan York — *PCB Lead*
Kyle Koch — *VHDL Lead*

Summary

Our work during this reporting period focused on the implementation phase of the modules that we completed designing previously. Work was done to finalize all of the control and timing signals in the KiCAD schematic for the memory drum, and we began laying out the PCB for this module. The control panel schematic and PCB layout were updated to use the improved buttons and switches we received. The KiCAD schematic and VHDL simulation of the individual control components and the clock module were completed. For our full VHDL simulation, more work was done to connect the different card reader components to the full memory and computation components. The memory was also updated so that the contents could be easily viewed for debugging.

Past Weeks Accomplishments

- Vance
  - For BDF with Kyle, completed the entire connection from Decimal Card input to 4-1 mux which leads to inner workings of ABC. Did the same thing with Binary Card input, then connected Binary Card output.
  - Modified drum VHDL files to have a memory file that is viewable before, during, and after simulation.
- Bryan
  - Continued working through the timing analysis of the Memory circuit to ensure proper timing of circuits.
  - Started in on the layout and looking at the sizing of the overall module.
  - Finalized the schematic and incoming control signals with Samuel.
- Kyle
  - Worked with Vance on the BDF file to make sure it was correct and looked like our diagram. Had to make many changes because we are only testing one of the six segments, not all six.
  - Implement the binary input and output units in VHDL, then test them to ensure they work. Also made the CSV files for decimal and binary so we can read in the stored values.
- Ryan
  - Tested our buttons and switches on breadboards, particularly focusing on debouncing methods and our circuit for mutually exclusive switches on the control panel

    - Used Fusion 360 to create versions of i281's switch holders for the custom lengths we will need for our boards (2 switches, 3 switches, etc.)
    - Imported these 3D models and the switch and button footprints from the i281 board into the control panel PCB design
    - Updated control panel schematic with simplifications based on i281's front panel and their switch and button circuits
    - Established layout of control panel PCB for peer review
- Samuel
    - Created VHDL simulations and KiCAD schematics for all of the control modules
    - Worked with Bryan on the timing analysis of the memory circuit
    - Worked on modelling the final assembly and choosing parts for it
    - Updated our system diagram with all control signals
- Gavin
    - Polished and wrapped up the final designs for the clock circuit including:
        - Technical schematic
        - VHDL code
    - Still pending the PCB layout and fabrication files finalization, but made great progress in this front.
    - Completed timing testing of the clock and process counter in VHDL to ensure functionality.

Pending Issues

- No pending issues

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Gavin Bunker	Polished clock circuit design, schematic, and VHDL. Timing test for clock	14	49
Ryan McFadden	Porting over i281 footprints and customizing their 3D prints, breadboard testing of switches and buttons, Control Panel schematic and PCB layout updates	9	42
Samuel Schroeder	VHDL and KiCAD for the control system, memory timing, final assembly modelling, and updating documentation	12	50
Vance Arnold	BDF Decimal/Binary Card input connection completed, Binary output connected, memory drum mid-simulation content viewing modification added.	8	44
Bryan York	Timing and layout work on the memory drum	8	39
Kyle Koch	Work with Vance on BDF, Binary input and output of your design, and overall design changes	7	39

Plans for Coming Week

- Vance and Kyle
    - Add any additional control signals to BDF and individual modules.
    - Work on converting BDF to VHDL and begin simulating a two-equation system, showing input and output.

- Bryan
    - Layout the memory drum module and send it to ETG for production.
- Ryan
    - Make adjustments to the control panel's PCB layout based on feedback from Dr. Stoychev and route the board in order to send to ETG for production
- Samuel
    - Finish the KiCAD schematic for the control system
    - Test the VHDL of the control system
- Gavin
    - Work on the PCB layout for the clock circuit