EE / CprE / SE 4920 – sdmay26-12
ABC with Modern Components
Report 14

03/13/2026 – 03/26/2026
Client: Alexander Stoytchev
Faculty Advisor: Alexander Stoytchev

Team Members:

Gavin Bunker — *Technical Manual Lead*
Ryan McFadden — *Client Liaison, Recorder*
Samuel Schroeder — *Team Leader*
Vance Arnold — *Team Facilitator, Purchasing*
Bryan York — *PCB Lead*
Kyle Koch — *VHDL Lead*

Summary

During this reporting period, we completed, or nearly completed, most of the PCB modules for our final replica. The control panel module was completed and ordered; the clock was completed and just needs to be ordered; and the memory module is complete except for a few necessary changes we discovered during our review process. The control module schematic and VHDL simulation were completed, and the PCB has been started. The block diagram for the full software simulation was completed, converted to VHDL, and used to perform a system test of the drum clearing functionality.

Past Week's Accomplishments

- Samuel
  - Finished the KiCAD schematic and VHDL simulation for the control system
  - Started laying out the PCB in KiCAD
- Ryan
  - Finished PCB layout for Control Panel Module and submitted order to ETG
  - Began looking into sdmay25-29's code for card readers (both ESP32 and Android Apps)
- Vance
  - Finished Block Diagram for now and converted to VHDL
  - BDF conversion to VHDL optimized/fixed for Questasim simulation
  - Full simulation pipeline testbench created with clear drums correctly working, continuing towards the next step
- Kyle
  - Finished the changes to the input and output binary and decimal readers to work for only 5 bits instead of all 30.
  - Worked with Vance on the compilation errors with the BDF conversion to VHDL.
  - Had an issue with git ignore files and file locations, I fixed it to be able to simulate the overall design and help Vance work on the next steps
- Bryan
  - Route signals on the memory drum PCB
  - Review the schematic design against the block diagram
- Gavin
  - Finished PCB layout for Clock module

- Began investigating the final module for the computer that connects the Tablets to the rest of the computer via Bluetooth modules.

Pending Issues

- No pending issues

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Gavin Bunker	Finished Clock PCB and began investigating the final tablet module.	10	59
Ryan McFadden	Finished PCB layout for Control Panel, began looking into sdmay25-29's code for card readers	10	52
Samuel Schroeder	Creating the control system schematic, VHDL, and PCB	22	72
Vance Arnold	Finished work on BDF and VHDL conversion, Created full pipeline simulation testbench	12	56
Bryan York	Route signals on memory drum PCB	35	74
Kyle Koch	Finished input and output modules and worked with Vance on VHDL simulation	9	48

Plans for Coming Week

- Samuel
  - Finish laying out the control system PCB
- Vance & Kyle
  - Continue full simulation testbench and continue working through the test steps given by the client
  - Change the full VDHL file as needed
- Bryan
  - Finalize and submit PCB designs for the memory drum
- Ryan
  - Help with card reader PCBs
  - Update the card reader software from last team for 5 bits instead of 4 bits
- Gavin
  - Order the clock PCB
  - Begin designing card reader PCBs