EE / CprE / SE 491 – sdmay26-12
ABC with Modern Components
Report 2

09/24/2025 – 10/07/2025
Client: Alexander Stoytchev
Faculty Advisor: Alexander Stoytchev

Team Members:

Gavin Bunker — *Technical Manual Lead*
Ryan McFadden — *Client Liaison, Recorder*
Samuel Schroeder — *Team Leader*
Vance Arnold — *Team Facilitator, Purchasing*
Bryan York — *PCB Lead*
Kyle Koch — *VHDL Lead*

Summary

During this reporting period, our team's goal was to learn the prototyping and design process that we will be using throughout this project, understand the algorithm that the ABC used, and continue to learn about how the original ABC worked. Using the add/subtract module of the ABC as an example, team members implemented and tested breadboard prototypes of the module, continued refining their PCB schematic, and began work on writing VHDL simulations of the module. To better understand what the ABC did and the algorithm it used, each team member solved two systems of equations using Atanasoff's algorithm.

Past Week Accomplishments

- Samuel
  - Implemented my adder/subtractor circuit on a breadboard to have a physical prototype for testing. Tested this prototype to ensure it implements the same logic as the ABC module.
  - Solved two systems of three linear equations in three unknowns using my standard method and using Atanasoff's modified Gaussian elimination algorithm, so that I can better understand how the ABC solved systems of equations.
  - Re-read the section in the book (*The First Electronic Computer*) about converting the base-10 punch card input into binary signals, so that I have a better understanding of how this system works in preparation for our next client/advisor meeting. Specifically focused on how the binary conversion drum stored all of the binary versions of base-10 inputs.
  - Worked on polishing up my adder/subtractor PCB design by adding all I/O pins, organizing the schematic, and adding silkscreen labels for individual components. Ensured all design and rule checks passed.
- Ryan
  - Solved a system of three linear equations with three unknowns using both standard algebra and the ABC's modified Gaussian elimination algorithm to better understand how the ABC solved systems of linear equations
  - Developed breadboard prototype of adder/subtractor circuit and tested it
  - Wrote VHDL code for our adder/subtractor module
- Bryan

    - Troubleshot KiCad schematic and Layout to logically match the expected results of the Full Adder/Subtractor Module.
    - Constructed a Breadboard version of the full adder with IC's and basic electronic components. This included building the module, labeling important traces, and testing the output result.
    - Solved a system of three linear equations using the substitution, Gaussian elimination for matrices, and the ABC's Gaussian elimination method.
    - Created a Design Standards document for PCB design and production to be utilized by the whole team.
    - Created VHDL code script and test bench to test the full add/subtract module, and verified the functionality of the KiCad schematic I have made.
    - Brainstormed some ideas about possible team logos to use on all designs
- Kyle
    - Solved a system of three linear equations using the substitution, Gaussian elimination for matrices, and the ABC's Gaussian elimination method, which was requested by our Client.
    - I've completed my breadboard of a full adder, and it's ready to show to our advisor.
    - Started to put together a folder with all our basic structural VHDL digital logic blocks in so that we can start to build off of them for testing and verification of your circuit designs.
- Vance
    - Read through the modified ABC Gaussian elimination provided by the client. Solved two systems of three linear equations using the provided ABC modified Gaussian elimination algorithm. Verified results to ensure understanding of algorithm.
    - Began preparation and planning of a breadboard module of the full adder with basic electronic components and the ICs.
    - Built breadboard using IC's and basic electronic components.
    - Discussed and read through the process of ordering/purchasing parts for the project as part of new Purchasing role responsibilities.
    - Began designing of full adder in VHDL digital logic blocks to begin VHDL structural planning designs.
- Gavin
    - Implemented and tested the adder/subtractor on a breadboard, validated sum and difference with carry and borrow across test table.
    - Solved a system of three linear equations using standard algebra and the ABC modified Gaussian elimination to confirm understanding of the ABC algorithm.
    - Updated the adder/subtractor PCB to conform to our design standard, finalized I/O pinout, organized the schematic, and added silkscreen labels.
    - Managed parts procurement through ETG, updated the parts tracker, compared vendor pricing, checked equivalents and availability, confirmed lead times, and submitted the order.
    - Proofread/edited/provided comments and input on the design document

Pending Issues

- No pending issues.

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Gavin Bunker	Breadboard add/sub module building & testing, practice with gaussian elimination, PCB design to conform to standard, Parts ordering from ETG, design doc writing	11	22
Ryan McFadden	Practice with Gaussian algorithm, making breadboard prototype, programmed VHDL for ABC's full adder circuit	11	21
Samuel Schroeder	Breadboard prototype, practice with the ABC's algorithm, base conversion research, PCB design	15	26
Vance Arnold	Breadboard planning and completion, ABC Gaussian algorithm reading, Solved 2 systems of linear equation problems, Began research and reading of purchasing/ordering parts processes, began VHDL design	11	21
Bryan York	Breadboarding, PCB Standards Creation, Solved Linear Equations, and Brainstormed Team Logos and implemented VHDL code.	11	26
Kyle Koch	Breadboard, solving systems of liner equations and VHDL Standards research.	12	21

Plans for the Coming Week

- Complete the implementation of our design of the adder/subtractor module in structural VHDL.
- Use QuestaSim and the VHDL implementation to test our module design.
- Continue work on PCB design and standardization for the add/subtract module.