EE / CprE / SE 491 – sdmay26-12
ABC with Modern Components
Report 3

10/08/2025 – 10/14/2025
Client: Alexander Stoytchev
Faculty Advisor: Alexander Stoytchev

Team Members:

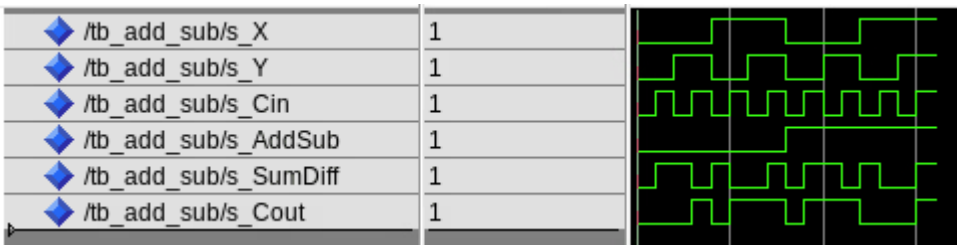
Gavin Bunker — *Technical Manual Lead*
Ryan McFadden — *Client Liaison, Recorder*
Samuel Schroeder — *Team Leader*
Vance Arnold — *Team Facilitator, Purchasing*
Bryan York — *PCB Lead*
Kyle Koch — *VHDL Lead*

Summary

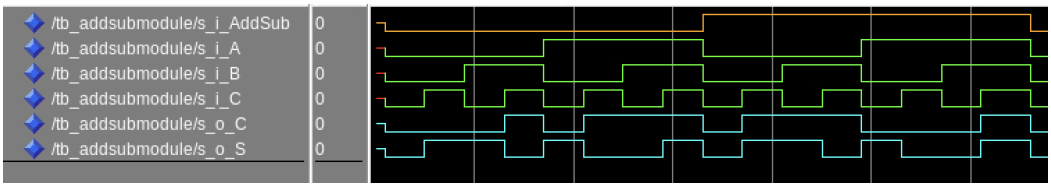
During this reporting period, our team's goal was to complete the design and prototyping process for the add/subtract module of the ABC, which involved making VHDL simulations of the model and testing these simulations with QuestaSim to verify the accuracy of our designs. We also worked to create a finished PCB design that will meet the space constraints of our plans for final assembly. Team members set up and configured our provided GitLab instance to better support our development process and hold all of our VHDL files.

Past Week Accomplishments

- Samuel
  - Constructed my logical design for the add/subtract module with structural VHDL. Created and ran a test bench on this simulation to verify the correctness of my logical design.



  - Set up our GitLab with appropriate settings to support our merge request review process. Added automated linting checks using pre-commit to ensure our VHDL code has a standard format. Set up our GitLab issues board and created labels to help us track the progress of each task.
  - Finished PCB design of the add/subtract module with proper pin spacing, standardizations, and an organized schematic.
- Vance
  - Constructed 2 and 3-input NAND and 2-input NOR modules in structural VHDL in QuestaSim. Constructed logical design for the add/subtract module with structural VHDL in QuestaSim. Created a custom tench bench and ran through all 16 input combinations to verify correctness of my design.

    - Set up GitLab locally and made the first push to include the add/sub module. Included folder of base modules that can be used in our further VHDL work.
- Bryan
    - Dove deeper into PCB modules and pin spacing and module area. Redesigned PCB module with space claim analysis, and to fit onto a standard breadboard. This second design can now fit two modules onto one breadboard. I also added female sockets to allow for easy connection above the modules as well.
    - Reviewed VHDL code and simulation to make everything into structural VHDL.
- Kyle
    - Reviewed my VHDL code and made sure it worked with a new and correct test bench using QuestaSim.
    - Then, I worked on double-checking others' VHDL code to ensure it was correct and followed the correct structural flow, rather than behavioral VHDL.
- Gavin
    - Organized and configured the team's GitLab repository.
    - Finalized the KiCad PCB design for the add/subtract module, ensuring proper pin spacing, adherence to standardization practices, and compatibility with the breadboard layout.
    - Drafted and refined the initial VHDL modules for the add/subtract design, aligning them with the project's structural VHDL conventions. Began initial draft of VHDL add/subtract design.
- Ryan
    - Finished developing and testing my VHDL design of the Add/Subtract Module. I created a test bench to test my module, and the results matched the ABC's truth table.
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    - Learned about using "do" files to compile and test VHDL modules more quickly, to be more efficient in our VHDL development and testing down the road
    - Uploaded my VHDL code to our team's Git repository

Pending Issues

- No pending issues.

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Gavin Bunker	GitLab organization and setup, finalize Kicad design, VHDL module drafting	4	26
Ryan McFadden	VHDL development and testing, GitLab configuration	3	24
Samuel Schroeder	VHDL simulation and verification of the add/sub module, GitLab configuration, and finished PCB design	6	32
Vance Arnold	VHDL design of NAND and NOR modules, and design and testing of add/sub module. Initial GitLab work.5	5	26
Bryan York	Created a new PCB module for the Adder/Subtractor module. Reviewed VHDL code.	5	31
Kyle Koch	VHDL checking and test bench creation for add/sub unit	5	26

Plans for the Coming Week

- Send in the Adder/Subtractor PCB Module to ETG for review.
- Begin documentation of the design and functionality of the Adder/Subtractor Module.
- Select and start researching the next modules to begin designing and prototyping.