EE / CprE / SE 491 – sdmay26-12
ABC with Modern Components
Report 6

10/29/2025 – 11/04/2025
Client: Alexander Stoytchev
Faculty Advisor: Alexander Stoytchev

Team Members:

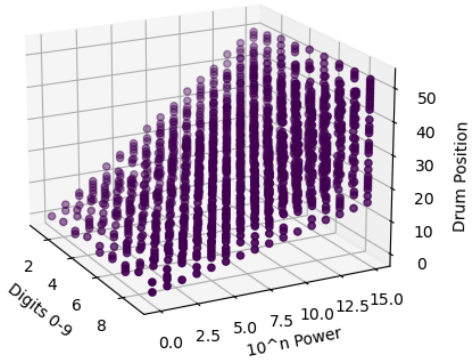
Gavin Bunker — *Technical Manual Lead*
Ryan McFadden — *Client Liaison, Recorder*
Samuel Schroeder — *Team Leader*
Vance Arnold — *Team Facilitator, Purchasing*
Bryan York — *PCB Lead*
Kyle Koch — *VHDL Lead*

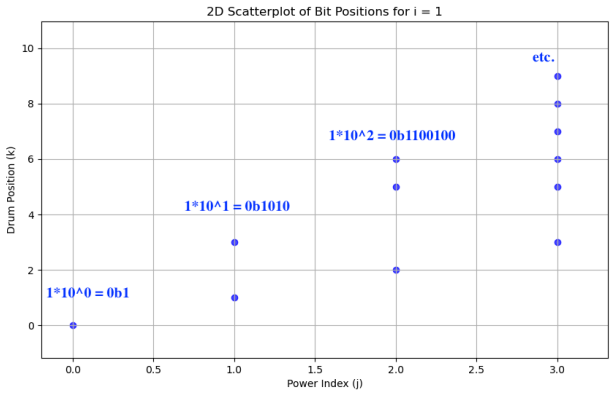
Summary

For this reporting period, our team focused on starting the design and prototyping process for each of the modules that were chosen at the end of the previous reporting period. While waiting for the necessary parts for the conversion drum, we created created visuals to better understand how the drum works. For the decimal output module we worked to create an initial circuit diagram and find which components we would want to use. We also worked to create a VHDL simulation of the clock circuit and added to our system design diagram.

Past Week Accomplishments

- Ryan
  - Worked with ETG to get software installed on lab computers to program EEPROM chips (still waiting for the chips we ordered to come in). Also came to a better understanding of how the binary conversion drum works and what values we are storing in the drum using matplotlib visualization.

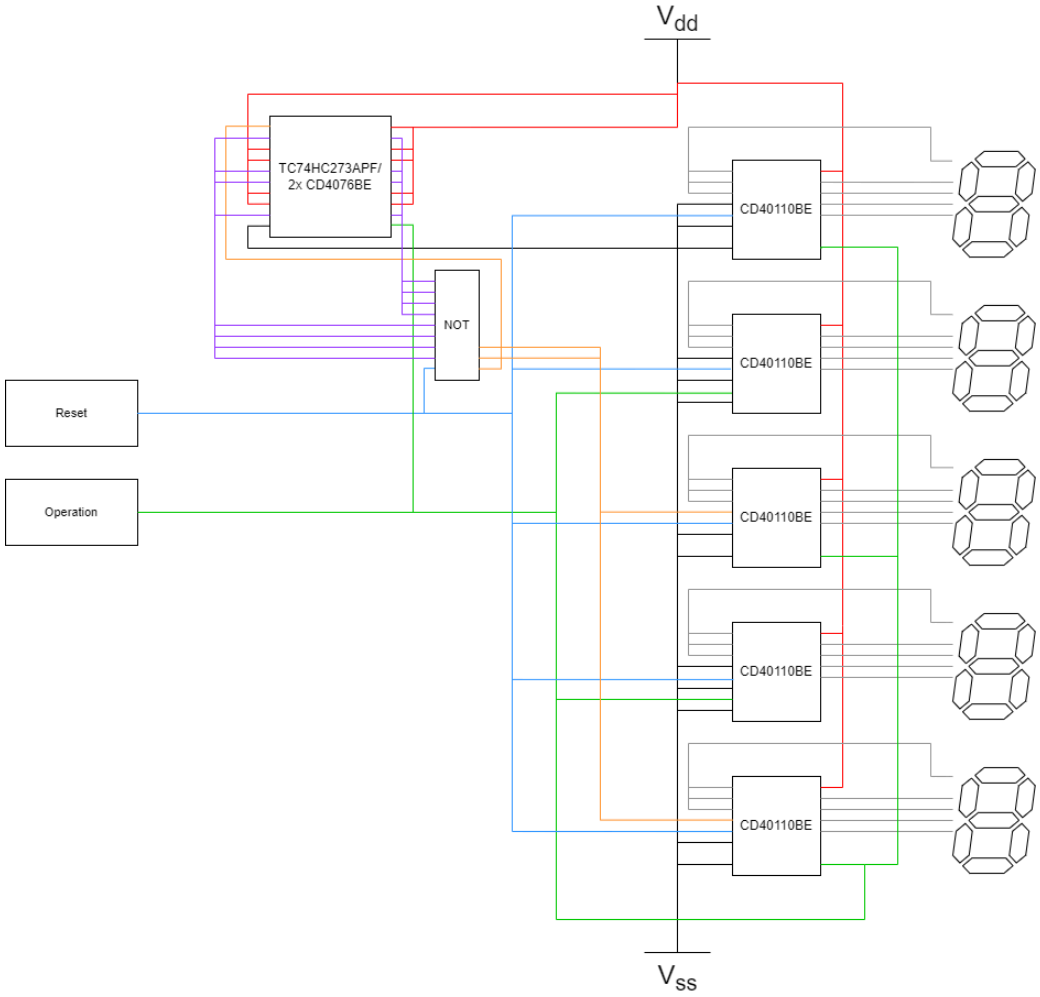




- Samuel
  - Used Atanasoff's 1940 paper, Berry's manual, and the 90s replica team's demo video to

analyze how the ABC's decimal output dials worked.

- Since there were two different implementations, I created a simulator script for each design to determine how the algorithm actually worked and how the dials were arranged.
- Created a preliminary circuit design for the decimal output module.



- Updated our system design diagram with the changes we made.

- Vance
  - Inventoried sdmay25-29 leftover parts and materials. This included finding online links and datasheets, counting quantities, and organizing in a spreadsheet. This info was sent to the client. Worked with ETG and ordered several parts for the project, including EEPROMs, counters, and various switches and connectors. Read through the clock circuit and seven-segment display lab documents, looking at parts, design, and ways to integrate aspects into our own project. Researched potential components and parts that may need to be ordered for the project.
- Kyle
  - Waiting on more details for the VHDL specifications and how we plan to implement them. In the meantime, I am trying to better understand how all the components of the ABC work and how we will implement them in VHDL. Then spent time trying to figure out some of the design mysteries of the ABC that have not been figured out.
  - Spent time to better understand the overview of the design drawn on the board by our client, as I had missed the meeting due to a work conflict.
- Gavin
  - Researched the clock module using the ABC manual/book and other open source projects online

    - Pulled from Git and generated initial VHDL code, using documents the client provided on generic modern clock circuits.
    - Maintaining code on the local machine until I am ready with the final product to minimize the number of times that I have to merge with main and deconflict
- Bryan
    - Looked into Binary to Decimal output displays and Seven Segment Displays. Looked into what chips we could use to take in 4 - 1 bit signals and output signals corresponding to the seven-segment display.
    - Soldered the first module for the Add-Subtract Module as the boards arrived.
    - Looked over the parts given to us by the previous senior design team, to see if any could be used for a segment display output.

Pending Issues

- We are still waiting for our EEPROMS and some other parts to arrive that we need to test components and designs.
- Need more details for the VHDL specifications and how we plan to implement them.

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Gavin Bunker	Surface-level research on the original clock module, initial skeleton coding of the clock module	5	43
Ryan McFadden	Getting EEPROM SW on lab computer, created binary conversion drum visualizations, printed archive diagrams for the team's reference	5	37
Samuel Schroeder	Historical analysis and initial design of the decimal output module. Design diagram updates.	7	52
Vance Arnold	Inventoried sdmay25-29 leftover parts in a spreadsheet. Ordered parts needed for upcoming module designs. Researched circuit design and future part/component orders.	5	41
Bryan York	Gathered part numbers for the segment display output and soldered the Adder Subtractor module.	7	53
Kyle Koch	Design and functionality of the ABC research, and understanding how to approach VHDL design of the system.	3	35

Plans for Coming Week

- Gavin: Implement the remaining VHDL clock as much as possible prior to the client meeting. Take notes in the appropriate technical manual section for documentation
- Ryan: Programming the EEPROM (once it arrives) and prototyping the binary conversion drum circuit
- Bryan and Samuel: Finalize an initial design for the decimal output module, create a KiCAD schematic of the design
- Kyle and Vance: Work on creating VHDL components that can be used for the full model