EE / CprE / SE 491 – sdmay26-12
ABC with Modern Components
Report 8

11/12/2025 – 11/18/2025
Client: Alexander Stoytchev
Faculty Advisor: Alexander Stoytchev

Team Members:

Gavin Bunker — *Technical Manual Lead*
Ryan McFadden — *Client Liaison, Recorder*
Samuel Schroeder — *Team Leader*
Vance Arnold — *Team Facilitator, Purchasing*
Bryan York — *PCB Lead*
Kyle Koch — *VHDL Lead*

Summary

As in the previous reporting period, our team continued working on the selected modules and soldering the add/subtract PCBs as we received parts for them. The decimal output module was redesigned to correct an error in the previous design and simplify the module, the PCB layout for the binary conversion module was adjusted to incorporate client feedback, and the clock was improved to support multiple speeds and thresholds. For the VHDL simulation, the input card module created last week was tested, and work on simulating the card outputs began.

Past Week Accomplishments

- Vance
  - Completed testing module of binary card input proof of concept in VHDL. Tested and verified with the client.
  - Created plan for testing module of output proof of concept in VHDL.
  - Further designs for ABC equation dataflow in VHDL developed.
  - Worked with ETG to get the correct parts ordered.
- Bryan
  - Re-designed the seven-segment display and select with a new chip set and select lines.
  - Added in preload option to the counter chip.
  - Changed seven-segment display chips to be common cathode.
  - Soldered as many components as possible to the printed Full Add Subtract Modules.
- Kyle
  - Work a little on the VDHL design for the output from the binary cards
  - Worked a little more on the soldering of my add/sub module, but still waiting on the sockets for the components to come in.
  - I had a lot of work for another class due to a huge lab presentation, so I didn't have a lot of time for senior design.
- Ryan
  - Did some planning for a new layout for the binary conversion drum based on Dr. Stoytchev's comments at our last meeting

    - Had a heavy workload with other classes this week, so I was not able to put a lot of time into senior design this week
- Samuel
    - Simulated the decimal output module design using Python, finding a design flaw that required a redesign of the module.
    - Redesigned the decimal output module to handle numbers with trailing zeros, e.g. 1000. Used the same simulation as the previous design to test and verify this design.
    - Worked more on the control signals and modules to determine which signals our replica needs for each operation, and to determine how we can implement the original ABC's control modules.
- Gavin
    - Reworking of the Clock VHDL
    - Research how to implement various clock speeds and thresholds
    - Finished soldering a second Add/Sub module (not including the IC sockets we don't have)

Pending Issues

- We are waiting for a new order of chip sockets to arrive so that we can finish assembling the add/subtract PCBs. For the first order of sockets, only 6 sockets were ordered instead of 6 packages of sockets.

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Gavin Bunker	Clock VHDL and how to implement various clock speeds and thresholds, finished soldering a second Add/Sub module	6	57
Ryan McFadden	Planned a new layout of the binary conversion drum PCB	1	48
Samuel Schroeder	Decimal output designing and testing, control modules planning and design.	5	63
Vance Arnold	Finished binary card input POC in VHDL, along with verified testing. Drew up plans for output POC. Ordered more parts for the project.	5	50
Bryan York	Soldered Full Adder Subtractor Modules and Re-Designed Seven Segment Modules.	6	71
Kyle Koch	Soldering and design with limited time due to other classes.	2	45

Plans for the Coming Week

- Prepare for our final presentation
- Organizing our parts cabinet
- Continue finishing our design document